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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/740,902	12/21/2000	Junichi Asada	201163US2S	6347

22850 7590 11/16/2004

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EXAMINER	
CHU, CHRIS C	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 11/16/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/740,902	ASADA, JUNICHI	
	Examiner	Art Unit	
	Chris C. Chu	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 July 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *28 - 31, 36 and 37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *28 - 31, 36 and 37* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Request for Continued Examination

1. A request for continued examination (RCE) under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on July 23, 2004 has been entered. An action on the RCE follows.

Response to Amendment

2. Applicant's amendment filed on July 23, 2004 has been received and entered in the case.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 28 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sugano et al. '888 in view of Oshino et al. (JP 63-107126).

Regarding claim 28, Sugano et al. discloses in e.g., Figs. 6, 7, 16 and 18 a semiconductor apparatus (e.g., 15d) comprising:

- a semiconductor device (e.g., 49d);
- a plurality of lead wires (lead wires that are adjacent on either side of the dummy lead wires 69c) connected to a plurality of connecting electrodes (58) formed on said semiconductor device (see e.g., the second figure of Fig. 18 wherein the lead wire to the right of dummy lead 69c is electrically connected to the electrode 58);
- at least a single dummy lead wire (69c) that is not electrically connected to said semiconductor device and does not include an outer lead portion by a common outer wiring path for electrically connecting said semiconductor device to an external circuit of said semiconductor device (while the dummy lead 69c may be deemed to have an "outer lead portion," because the lead is not electrically connected, Sugano et al.'s wiring structure does not include "an outer lead portion by a common outer wiring path *for electrically connecting said semiconductor device to an external circuit of said semiconductor device*");
- an insulating film (62c or 9c in Fig. 6 and column 5, lines 63 - 67) having an opening portion configured to accommodate said semiconductor device and to support said plurality of lead wires connected to the plurality of connecting electrodes of the semiconductor device and said at least the single dummy lead wire, said opening portion having a plurality of sides that define a perimeter of said opening portion; and
- a resin molding (8a, column 5, lines 59 – 61 and column 26, lines 47 – 57) configured to cover a connecting portion between tip portions of the plurality of lead wires and the plurality of connecting electrodes and the tip portion of said at least the single dummy lead wire within the opening portion of said insulating film,

- wherein said at least a single dummy lead wire (69c) is arranged in a space defined by two adjacent lead wires (lead wires that are adjacent the dummy lead wires 69c and the lead wires 67c and 68c) of said plurality of lead wires so that a length of said space is at least twice a minimum pitch between adjacent lead wires of said plurality of lead wires, and the two adjacent lead wires being provided on one side of said plurality of sides of the insulating film to define the space on the one side of the insulating film.

Sugano et al. discloses the claimed invention except for a tip portion of the at least the single dummy wire extending over the semiconductor device. Oshino et al. teaches in e.g., Fig. 1 a tip portion of at least a single dummy wire (5A) extending over a semiconductor device (3). Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Sugano et al. by using the tip portion of the at least a single dummy wire extending over the semiconductor device as taught by Oshino et al. The ordinary artisan would have been motivated to modify Sugano et al. in the manner described above for at least the purpose of uniformly applying the pressure or heat of the bonding tool to the connecting parts of the electrodes and the leads (abstract, lines 1 – 4 from the bottom).

Regarding claim 29, Sugano et al. discloses in e.g., Figs. 6, 7, 16 and 18 a semiconductor apparatus (e.g., 15d) comprising:

- a semiconductor device (e.g., 49d);
- a plurality of lead wires (lead wires that are adjacent the dummy lead wires 69c and the lead wires 67c and 68c) connected to a plurality of connecting electrodes (58) formed on said semiconductor device;

- at least a pair of dummy lead wires (69c) that are not electrically connected to said semiconductor device and do not include an outer lead portion for electrically connecting said semiconductor device to an external circuit of said semiconductor device;
- an insulating film (62c or 9c in Fig. 6 and column 5, lines 63 - 67) having an opening portion configured to accommodate said semiconductor device and to support said plurality of lead wires connected to the plurality of connecting electrodes of the semiconductor device and said at least the pair of dummy lead wires, said opening portion having a plurality of sides that define a perimeter of said opening portion; and
- a resin molding (8a, column 5, lines 59 – 61 and column 26, lines 47 – 57) configured to cover a connecting portion between tip portions of the plurality of lead wires and the plurality of connecting electrodes and a tip portion of said at least the pair of dummy lead wires within the opening of said insulating film;
- wherein one and the other of said at least the pair of dummy lead wires (69c) provided on one side and an opposite side of said plurality of sides of said insulating film, respectively, each of the one and the other of said at least the pair of dummy lead wires being arranged in corresponding first and second spaces defined by first and second two adjacent lead wires (lead wires that are adjacent the dummy lead wires 69c and the lead wires 67c and 68c) of said plurality of lead wires, respectively, so that a length of each said first and second spaces is at least twice a minimum pitch between adjacent lead wires of said plurality of lead wires, said first two adjacent lead wires being provided on said one side of said insulating film to define said first space

on said one side of said insulating film, and said second two adjacent lead wires being provided on said opposite side of said insulating film to define said second space on said opposite side of said insulating film.

However, Sugano et al. does not disclose the location of the one of the pair of dummy lead wires being placed on the opposite side surface of the plural side surfaces of said insulating film to correspond to the other one of the pair of dummy lead wires and a tip portion of the at least the single dummy wire extending over the semiconductor device. Oshino et al. teaches in e.g., Fig. 1 a location of one (5A) of a pair of dummy lead wires (5A at the right side and the top 5B at the left side) being on the opposite side surface of the plural side surfaces of a insulating film (6) to correspond to the other one (the top 5B at the left side) of the pair of dummy lead wires (5A at the right side and the top 5B at the left side) and a tip portion of at least a single dummy wire (5A) extending over a semiconductor device (3). Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Sugano et al. by placing the one of the pair of dummy lead wires being placed on the opposite side surface of the plural side surfaces of said insulating film to correspond to the other one of the pair of dummy lead wires and using the tip portion of the at least a single dummy wire extending over the semiconductor device as taught by Oshino et al. The ordinary artisan would have been motivated to modify Sugano et al. in the manner described above for at least the purpose of uniformly applying the pressure or heat of the bonding tool to the connecting parts of the electrodes and the leads (abstract, lines 1 – 4 from the bottom).

5. Claims 30 and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sugano et al. and Oshino et al. as applied to claims 28 and 29 above, and further in view of Walter '640.

Sugano et al. and Oshino et al. disclose the claimed invention except for the thickness of the semiconductor chip being approximately 50 μm. Walter teaches in e.g., Fig. 1, column 1, lines 41 – 45 and column 3, lines 42 – 43 a semiconductor chip (30) in which a semiconductor device is formed has a thickness of approximately 50 μm. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to further modify Sugano et al. by using the thickness of the semiconductor chip to be approximately 50 μm as taught by Walter. The ordinary artisan would have been motivated to further modify Sugano et al. in the manner described above for at least the purpose of (1) increasing heat dissipation, (2) reducing size and weight of the package, (3) providing an increased density of conductive lines and (4) providing microscopic thicknesses of the chips (column 1, lines 48 – 49).

6. Claims 36 and 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sugano et al. and Oshino et al. as applied to claims 28 and 29 above, and further in view of Lamson et al. '220.

Sugano et al. and Oshino et al. disclose the claimed invention except for a tip portion of the at least two dummy wires extending over the semiconductor device and the tip portions of the at least two dummy wires being connected to each other on the semiconductor device. Lamson et al. teaches in e.g., Fig. 3 a tip portion of at least two dummy wires (dummy wires at the top of the Fig. 3 to form " ⊔ "shape) extending over a semiconductor device (40) and the tip portions of the a least two dummy wires being connected to each other on the semiconductor device.

Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to further modify Sugano et al. by using the " ⊔ "shaped dummy wires for the tip portion of the at least two dummy wires extending over the semiconductor device and for the connected tip portions of the two dummy wires the as taught by Lamson et al. The ordinary artisan would have been motivated to further modify Sugano et al. in the manner described above for at least the purpose of (1) preventing the insulating film from peeling off from the semiconductor chip, (2) increasing in the number of points of contact between the insulating film and the chip, (3) increasing heat dissipation efficiency as a method of increasing the reliability of metal leads, (4) increasing dispersion of stress, (5) reducing turbulence in the flow of resin to decrease voids when the resin is injected on the surface of the package and (6) providing added support to the encapsulated package (column 4, lines 1 – 2).

Response to Arguments

7. Applicant's arguments with respect to claims 28 and 29 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chris C. Chu whose telephone number is 571-272-1724. The examiner can normally be reached on 11:30 - 8:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 517-272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chris C. Chu
Examiner
Art Unit 2815

c.c.
11/5/04 2:38:08 PM

GEORGE ECKERT
PRIMARY EXAMINER